REMARKS

Applicants have amended the written specification as indicated above. These amendments correct minor grammatical and/or labeling errors within the application as filed. Care has been taken to avoid the introduction of new matter. The Examiner is respectfully requested to approve these amendments.

Claims 1-9, 11-20, 22-31 and 33-36 were previously pending in this application. By this amendment, Applicant is canceling claims 2, 3, 5, 13, 14, 16, 24, 25 and 27 without prejudice or disclaimer. Claims 1, 4, 6-9, 11, 12, 15, 17-20, 22, 23, 26, 29, 31 and 33 have been amended. As a result claims 1, 4, 6-9, 11, 12, 15, 17-20, 22, 23, 26, 28-31 and 33-36 are pending for examination with claims 1, 9, 12, 20, 23 and 31 being independent claims. No new matter has been added.

1. Clarification of Claims

Applicants have made a clarifying amendment to claims 1, 4, 6, 7, 8, 9, 11, 12, 15, 17, 18, 19, 20 and 22 by including the phrase "at least one" in all descriptions of the "at least one processor." This amendment was made so that all claims would be consistent and have proper antecedent basis. This amendment is not intended to narrow the scope of the claims in any way.

2. Rejections Under 35 U.S.C. §103

The Office Action rejects claims 1-3, 5, 12-14, 16, 23-25, and 27 under 35 U.S.C. §103(a) as being unpatentable over Razban, U.S. Patent No. 5,289,587 in view of Swoboda, U.S. Patent No. 5,828,824. Applicants respectfully traverse this rejection.

2.1 Discussion of Razban

As discussed in the Applicants' previous response, Razban is directed to a method for providing a microprocessor's program counter value external to a device on a dedicated bus so that an external in-circuit emulator system can generate a list of executed instruction addresses (col. 1, lines 17-21). In-circuit emulators (or ICE systems, as are known in the art) are a combination of external software and hardware used to design and troubleshoot software

programs executing on a target microprocessor or controller. Razban provides a virtual program counter value to an external ICE system via a dedicated external bus 30 (col. 4, lines 35-41; col. 4, line 66 - col. 5, line 4). Razban eliminates the conventional requirement of monitoring system bus traffic and attempting to extract and reconstruct the instruction execution sequence (Abstract, col. 2, lines 45-57).

2.2 Discussion of Swoboda

Swoboda teaches a method for debugging an integrated circuit containing multiple modules using extended operating modes, with particular attention paid to large scale integrated circuits (Abstract; col. 1, lines 7-10). Swoboda is intended to provide more advanced debugging and production test features than the IEEE standard 1149.1-1990 "Standard Test Access Port and Boundary Scan Architecture" (col. 6, lines 24-27; col. 7, lines 14-16). According to Swoboda, improved debugging and test features are achieved by incorporating four extensions into the IEEE standard, including debug facilities, multiple scan technologies, trigger channels, and extended operating modes, i.e. operating modes not provided by the IEEE Standard (col. 7, lines 19-24).

Debug facilities, operable in multiple modes, are provided to allow control of the execution flow of an application program, and to allow the modification of particular system elements (col. 7, lines 25-44). A debug environment is used to allow the debugging of a system in which there is a CPU core (col. 8, lines 50-54). In Figure 1 Swoboda teaches an integrated circuit debug environment that includes a debug host 100, access adapter 102, and target system 104 (col. 8, lines 51-56). Figures 2-5 provide details of the target system 104. In particular, with regard to Figure 2, there is provided a debugger/test controller 206 which performs debugging actions on the subsystem components, including CPU core 208a (col. 9, lines 35-39). The debugger/test controller functions as the emulation and test interface of a module to the IEEE interface (Table 1).

2.3 Claims 1, 12 and 23 Patentably Distinguish Over the Combination of Razban and Swoboda

Claim 1, as amended, incorporates all the limitations of previous claims 1-3. Claim 1 is directed toward a microcomputer, and recites that the microcomputer comprises at least one

processor, a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit, a system bus coupling the at least one processor and debug circuit, and a communication link coupling the at least one processor and debug circuit, wherein the at least one processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the at least one processor. Claim 1 additionally recites that the program counter value has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the at least one processor, and the at least one **processor is further configured to transmit to the debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction.**

As stated above, Razban provides a program counter external to a device on a dedicated bus. Swoboda discloses an improvement on an IEEE debug interface. Razban and Swoboda do not teach or suggest a microcomputer comprising, *inter alia*, at least one processor, wherein the at least one processor is configured to transmit to the debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction.

The Office Action asserts that Razban discloses a microprocessor that will trap an instruction if an exception occurs while executing the instruction (Office Action, p. 3, paragraph 3). The Office Action implies that the occurrence of an exception in the system of Razban indicates the status of a computer instruction. Trapping an instruction if an exception occurs is not the same as transmitting to a debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction. In the system of Razban an exception may occur when executing an instruction, but there is no disclosure of a processor transmitting to a debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction. Razban does not suggest this feature of claim 1. Likewise, Swoboda does not disclose this feature of claim 1. Accordingly, claim 1 distinguishes over the combination of Razban and Swoboda. Thus, withdrawal of the rejection of claim 1 under 35 U.S.C. §103(a) is respectfully requested.

Claims 4, 6-8, 11 and 34 depend from claim 1 and are allowable for at least the same reasons.

Claim 12, as amended, recites a microcomputer comprising at least one processor, a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit, a system bus coupling the at least one processor and debug circuit, means for transmitting to the debug circuit in real time, and a program counter value indicating the program counter of the at least one processor. Claim 12 further recites the limitation wherein the program value counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the at least one processor, and wherein the at least one **processor includes means for transmitting to the debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction.**

As discussed above with respect to claim 1, nowhere do Razban or Swoboda disclose a microcomputer comprising, *inter alia*, at least one processor, wherein the at least one processor includes means for transmitting to the debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction. Accordingly, claim 12 patentably distinguishes over the combination of Razban and Swoboda. Thus, withdrawal of the rejection of claim 12 under 35 U.S.C. §103(a) is respectfully requested.

Claims 15, 17-19, 22 and 35 depend from claim 12 and are allowable for at least the same reasons.

Claim 23, as amended, recites a method for transferring information between a processor and a debug circuit of a microcomputer, wherein the processor and debug circuit are implemented on a same integrated circuit. The method comprises steps of transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor, wherein the program counter value has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor. The method further comprises a step of transmitting to the debug circuit a status indicating that a computer instruction in the writeback stage is a valid computer instruction.

As discussed above in connection with claims 1 and 12, Razban and Swoboda do not teach or suggest a method for transferring information between a processor and a debug circuit of a microcomputer comprising, *inter alia*, a step of transmitting to the debug circuit a status

indicating that a computer instruction in the writeback stage is a valid computer instruction. Accordingly, claim 23 patentably distinguishes over the combination of Razban and Swoboda. Thus, withdrawal of the rejection of claim 23 under 35 U.S.C. §103(a) is respectfully requested.

Claims 26, 28-30, 33 and 36 depend from claim 23 and are allowable for at least the same reasons.

The disclosures of Razban and Swoboda are discussed above. Mann discloses a system with an on-chip trace memory that has locations available for storing trace information. The trace information indicates the execution flow of instructions executed by a processor of the system (Abstract). An executable thread can be traced via a debug port when the processor is supplied with an indication of which executable thread to trace (Abstract). The processor will then provide trace information upon the start of the executable thread (Abstract).

In Figure 1 Mann shows a host system H that is connected to a target system T via a serial link 110 (col. 5, lines 55-60). The target system T comprises a system memory 106, processor core 104 and a debug port 100. The processor core 104 and debug port 100 are within an embedded processor device 102. The processor device 102 is shown in detail in Figure 2 (col. 5, lines 40-col. 6, line 10). Within the processor device 102 of Figure 2 is trace control circuitry 218 and trace memory 200, which provide trace information used to reconstruct the flow of executed instructions in the processor core 104 (col, 6, lines 12-15).

Claim 9, as amended, is directed to a microprocessor comprising at least one processor, a debug circuit wherein the at least one processor and debug circuit are implemented on a same integrated circuit, a system bus coupling the at least one processor and debug circuit, and a communication link coupling the at least one processor and debug circuit, wherein the at least one processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the at least one processor. Claim 9 further recites that the **debug circuit is adapted to generate trace information including the program counter.**

Mann does not teach or suggest a microprocessor comprising, *inter alia*, a debug circuit, wherein the debug circuit is adapted to generate trace information. The Office Action, in regard to the rejection of claim 9, states that Mann discloses a trace memory that has a plurality of

locations for storing trace information that indicates execution flow of a plurality of instructions in the processor. However, Applicants point out that a trace memory that stores trace information is not a debug circuit that generates trace information including a program counter. The trace memory of Mann does not generate trace information. Thus, claim 9 patentably distinguishes over the combination of Razban, Swoboda, and Mann. Accordingly, withdrawal of the rejection of claim 9 under 35 U.S.C. §103(a) is respectfully requested.

Claim 20, as amended, recites a microcomputer comprising at least one processor, a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit, a system bus coupling the at least one processor and debug circuit, and means for transmitting to the debug circuit in real time, a program counter value indicating the program counter of the at least one processor. Claim 20 further recites the limitation wherein the **debug circuit includes means for generating trace information including the program counter**.

As discussed above, in connection with claim 9, neither Razban, Swoboda, or Mann teach or suggest a microcomputer comprising, *inter alia*, at least one processor and a debug circuit, wherein the debug circuit includes means for generating trace information including the program counter. Thus, claim 20 patentably distinguishes over the combination of Razban, Swoboda, and Mann. Accordingly, withdrawal of the rejection of claim 20 under 35 U.S.C. §103(a) is respectfully requested.

Claim 31, as amended, recites a method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit. The method comprises the steps of transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor. The method further comprises a step whereby the **debug circuit generates trace information including the program counter**.

As discussed above, in connection with claims 9 and 20, nowhere do Razban, Swoboda, or Mann teach or suggest a method for transferring information between a processor and a debug circuit of a microcomputer, wherein, *inter alia*, the method comprises a step whereby the debug circuit generates trace information including the program counter. Thus, claim 31 patentably

distinguishes over the combination of Razban, Swoboda, and Mann. Accordingly, withdrawal of the rejection of claim 31 under 35 U.S.C. §103(a) is respectfully requested.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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